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#### ORIGINAL RESEARCH PAPER

# A bidirectional hybrid switched inductor converter with wide voltage conversion range

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#### Abstract

A bidirectional hybrid switched inductor converter (BHSI) is proposed in this paper. The converter uses an inductor switching cell in order to achieve a wide voltage conversion range, smaller passive components, and lower stress on the active devices. Apart from these advantages, the introduction of the additional inductor in the switching cell does not increase the complexity of the control structure, as is usually the case with other topologies with multiple components. The BHSI is compared, in terms of inductor/capacitor energies and total device stress, to other state-of-the-art topologies and its advantages are highlighted. Two 3 kW prototypes were built, using Si-MOSFETs and GaN-FETs, in order to analyse their performances from the efficiency point of view, and to validate the theoretical findings. The stability analysis of the converter is performed and tested in a supercapacitor storage application, resulting in a good operation in both charge and discharge modes.

## 1 | INTRODUCTION

With the increase of microgrid integration and popularity of electrical vehicles, modern effective storage solutions are required. Modern storage elements have different characteristics in terms of energy and power density. Therefore an effective combination/coordination between them is generally put in place so that the overall performance of the storage system is optimized [1-3].

A storage element that is becoming more prevalent, the supercapacitor, is gaining attraction due to its better energy density, close to that of Li-ion batteries, much greater power density, and an increased durability [4]. Moreover, new technologies are currently under development for supercapacitors to further increase their performances [5–7].

In order to achieve a good energy storage utilization of supercapacitors, a wide range of voltage conversion during charge/discharge modes is required since the stored energy in any capacitor is proportional to the squared voltage on the device. Due to the fact that the supercapacitor is often used in combination with a conventional battery, the interface converters do not usually require galvanic isolation [8, 9].

To achieve a wide voltage conversion ratio, converter configurations make use of multiple passive components within fairly complex circuits [10–16], multilevel structures [17–19], switched capacitor or inductor cells in hybrid [20, 21] or extendable structures [22–26], or even multiple cascaded converters [27]. A disadvantage of these converters is that the larger number of passive components results in an increase in the complexity of control and reduction of the power density of the system, as presented in [20, 28].

This paper proposes a bidirectional hybrid switched inductor converter (BHSI), presented in Figure 1 [29]. The proposed circuit presents a hybrid structure as it uses a switched inductor cell that helps to achieve better characteristics, while using only three switches.

The main advantages are (i) a wider voltage conversion ratio, (ii) passive component size reduction, and (iii) active devices stress reduction. Apart from these advantages, the two identical inductors are dynamically characterized by only one state variable, as their currents are equal, therefore (iv) a simpler controller can be utilized. The BHSI schematic stems from the hybrid unidirectional switched inductor converters, presented either in boost [30] or buck [31] topologies.

The paper presents the BHSI steady-state operation in Section 2, with a detailed comparison to other topologies. The dynamic analysis from Section 3 provides information for controller design and overall stability. The theoretical analysis is

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FIGURE 1 Topology of the BHSI converter



**FIGURE 2** Equivalent schematic of BHSI during  $t_{on}$  interval ( $S_1$  is turned ON while  $S_2$  and  $S_3$  are turned OFF)

validated experimentally in Section 4 using two prototypes: using conventional MOSFET transistors and with GaN devices. Section 5 concludes the paper. The Appendix at the end present information regarding the dynamic model of the converter and information for comparison required in Section 2.

#### 2 | BHSI OPERATION

## 2.1 | Operation analysis

The BHSI converter from Figure 1 resembles a conventional bidirectional buck/boost converter with an additional switched inductor cell (consisted of  $L_1$ ,  $L_2$ ,  $S_2$ ,  $S_3$ ) at the low voltage output ( $V_L$ ). The topology uses three transistors that require one driving signal (applied to  $S_1$  and inverted for  $S_2$ ,  $S_3$ ), and two identical inductors.

The converter is analysed under continuous conduction mode (CCM) of operation, because of the simplicity to maintain this operating mode while using synchronous rectification. Additionally, the controller does not need a different tuning by avoiding DCM, and the efficiency is not necessarily affected [32].

The equivalent circuits for the two switching periods,  $t_{on}$  and  $t_{off}$ , are presented in Figures 2 and 3, respectively.

As depicted here, the two inductors from the switched cell are connected in series between the two inputs ( $V_L$  and  $V_H$ ) during  $t_{on}$ , and in parallel during  $t_{off}$ .

The current after the inductor cell (i.e.  $i_L + i_{CL}$ ) is, therefore, either, equal to, or double of the current through one inductor. The main theoretical waveforms presented in Figure 4 summarize the operation of the BHSI.



**FIGURE 3** Equivalent schematic of BHSI during  $t_{off}$  interval ( $S_1$  is turned OFF while  $S_2$  and  $S_3$  are turned ON)



FIGURE 4 Theoretical waveforms of the BHSI for step-down operation

The voltages on the two inductors ( $v_{L1}$  and  $v_{L2}$ ) are expressed from Figures 2 and 3, for the two switching periods:

$$\begin{cases} t_{on} : v_{L1} + v_{L2} = V_H - V_L \Leftrightarrow v_{L1} = \frac{V_H - V_L}{2}, \\ t_{off} : v_{L1} = v_{L2} = -V_L. \end{cases}$$
(1)

By applying the volt-second balance, the duty cycle (D) and conversion ratio can be determined:

$$\langle v_{L1} \rangle = \langle v_{L2} \rangle = D \cdot \frac{V_H - V_L}{2} + (1 - D) \cdot (-V_L) = 0, \quad (2)$$

$$D = \frac{2 \cdot V_L}{V_H + V_L} \Leftrightarrow V_L = V_H \cdot \frac{D}{2 - D}.$$
 (3)

#### 2.2 | Sizing of passive components

The initial part in design of the BHSI comprised the calculation of the required passive components. The resulting equations are also used as comparison metrics, as presented in the next section. In order to calculate one of the inductors, the nominal inductor current is calculated from  $I_{I}$ :

$$I_{L1} = I_L \cdot \frac{1}{2 - D} = \frac{V_L + V_H}{2 \cdot V_H} \cdot I_L.$$
 (4)

The inductance is obtained by considering a constant current ripple ratio, a common design parameter in converters [33], expressed as:

$$r_i = \frac{\Delta i_{L1}}{I_{L1}},\tag{5}$$

where  $\Delta i_{L1}$  is the inductor current ripple (Figure 4).

From the inductance volt-current dependency and Equations (4) and (5), the following expression is derived:

$$L_{1} = \frac{2 \cdot V_{H} \cdot V_{L} \cdot (V_{H} - V_{L})}{r_{i} \cdot f \cdot I_{L} \cdot (V_{L} + V_{H})^{2}}.$$
 (6)

The total inductor energy, as it is proportional to the size of the inductors and costs, is used for comparing the BHSI to other topologies and is calculated using:

$$W_{LTot} = 2 \cdot W_{L1}, \tag{7}$$

considering  $L_1$  and  $L_2$  are identical.

From (6),  $W_{L1}$  is calculated:

$$W_{L1} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{4 \cdot r_i \cdot f \cdot V_H}.$$
 (8)

Similar to (5), a voltage ripple ratio is used:

$$r_{\nu} = \frac{\Delta \nu_{CL}}{V_{CL}} = \frac{\Delta \nu_{CH}}{V_{CH}},\tag{9}$$

where  $\Delta v_{CL}$  and  $\Delta v_{CH}$  are the capacitor voltage ripples for the  $C_L$  and  $C_H$  capacitors, respectively (Figure 4).

The capacitor values are calculated assuming that the AC component of the low voltage side  $(I_L)$  and the high voltage side  $(I_H)$  currents are flowing entirely through the capacitors.

The currents flowing through  $C_L$  and  $C_H$  during the  $t_{on}$  interval are extracted from Figure 2, and the following relations are used to describe the discharge of the capacitors:

$$C_L \cdot \frac{dv_{CL}}{dt} = i_{L1} - I_L, \tag{10}$$

$$C_H \cdot \frac{dv_{CH}}{dt} = I_H - i_{L1}.$$
 (11)

Equations (10) and (11) are expressed in integral form to calculate the capacitances:

$$C_{L} = \frac{1}{-\Delta v_{CL}} \int_{0}^{I_{out}} (i_{L1} - I_{L}) dt, \qquad (12)$$

$$C_{H} = \frac{1}{-\Delta v_{CH}} \int_{0}^{i_{on}} (I_{H} - i_{L1}) dt.$$
(13)

Finally, the two capacitances are determined as:

$$C_L = \frac{I_L \cdot (V_H - V_L)}{r_v \cdot f \cdot V_H \cdot (V_H + V_L)},\tag{14}$$

$$C_{H} = \frac{I_{L} \cdot V_{L} \cdot (V_{H} - V_{L})}{r_{\nu} \cdot f \cdot {V_{H}}^{2} \cdot (V_{H} + V_{L})}.$$
(15)

The energies of the capacitors are calculated as follows:

$$W_{CL} = \frac{I_L \cdot V_L^2 \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot V_H \cdot (V_H + V_L)},$$
 (16)

$$W_{CH} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_{\nu} \cdot f \cdot (V_H + V_L)}.$$
 (17)

Similar to the total inductor energy, the total capacitor energy is used for comparing the BHSI to other converters, in terms of total capacitor volume or costs. The total capacitor energy for BHSI is given by:

$$W_{CTot} = W_{CH} + W_{CL} = \frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_v \cdot f \cdot V_H}.$$
 (18)

It is important to note that if electrolytic capacitors are used, the sizing factor should be based on the maximum RMS, as the values calculated in (14) or (15) might result in capacitors with insufficient current capabilities.

Another element used for comparing the converters, is the total active switch stress, S, defined in [34] as:

$$S = \sum_{j=1}^{3} V_{Sj} \cdot I_{Sj},$$
 (19)

where  $V_{Sj}$  and  $I_{Sj}$  are either the peak or RMS voltage and current, respectively, on the *j*th transistor. Considering that  $r_j$  has low values, the average current during conduction time is used as an approximation for its RMS value to simplify the calculations.

The total active switch stress is used to assess the overall switch losses or switch costs, because the number of switches alone in a converter might be insufficient for evaluating its performances.

For the BHSI, the transistor voltages and currents are:

$$V_{S1}/2 = V_{S2} = V_{S3} = (V_H + V_L)/2,$$
 (20)

$$I_{S1} = I_{S2} = I_{S3} = I_{L1} = \frac{I_L \cdot (V_H + V_L)}{2 \cdot V_H}.$$
 (21)

ies components summary
topolog
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nd other
BHSI a
TABLE 1

		No. of 6	elements		Voltage stress				Prototype s	pecifications			
Converter (x)	Voltage ratio $V_L/V_H$	Sw.	Г	U	$\mathbf{s}_1$	$\mathbf{S}_2$	S <sub>3</sub>	$S_4$	$V_{H}[V]$	$V_{L}$ [V]	$P_{in}$ [kW]	$f^{ m [kHz]}$	eff. [%]
1. Buck/boost	D	2	1	2	$V_{H}$	$V_{H}$					I		
2. BHSI	$\frac{D}{2-D}$	3	2	2	$V_H + V_L$	$\frac{V_H + V_L}{2}$	$\frac{V_H+V_L}{2}$		300	70	3	40	98
3. [20]	idem 2.	6	2	4	$\frac{V_H + V_L}{2}$	$\frac{V_H + V_L}{2}$	$\frac{V_H + V_L}{2}$		400	50	2	20	I
4. $[14]^{a}$	idem 2.	3	2	4	$\frac{V_H - V_L}{2}$	$\frac{V_H + V_L}{2}$	$\frac{V_H + V_L}{2}$		300	48	0.5	30	92
5. [36] <sup>b</sup>	idem 2.	4	2	2	$V_H + V_L$	$\frac{V_H + V_L}{2}$	$V_H + V_L$	$\frac{V_H + V_L}{2}$	100	20	0.1	50	98
6. [37]	idem 2.	3	2	4	$\frac{V_H + V_L}{2}$	$\frac{V_H + V_L}{2}$	$\frac{V_H + V_L}{2}$		240	120	0.3	20	96
7. [27]	$D^2$	4	7	3	$\sqrt{V_H \cdot V_L}$	$\sqrt{V_H \cdot V_L}$	$V_H$	$V_{H}$	64	12	0.05	100	
8. [11]	idem 7.	4	7	3	$V_{H}$	$\sqrt{V_H \cdot V_L}$	$\sqrt{V_H \cdot V_L}$	$\sqrt{V_H \cdot V_L}$	250	25	0.16	30	76
9. [23]	idem 7.	4	2	3	$V_{H}$	$\sqrt{V_H \cdot V_L}$	$V_{H}$	$\sqrt{V_H \cdot V_L}$	400	40	0.5	50	97
10. [24] <sup>c</sup>	idem 7.	4	7	ŝ	$\sqrt{V_H \cdot V_L}$	$\frac{V_{H}}{\sqrt{V_{H}\cdot V_{L}}}$	$V_{H}$	$\sqrt{V_H \cdot V_L}$	85	10		40	
11. [9]	idem 7.	3	2	3	$\sqrt{V_H \cdot V_L}$	$V_{H}$	$V_H$		200	24	0.2	15	89
12. [17] <sup>d</sup>	$\frac{D^2}{D^2 - D + 1}$	4	2	4	$\sqrt{V_L}(\sqrt{k} + \sqrt{V_L})$	$\frac{7}{H})/2$	$V_H - V_L$	$V_H - V_L$	210	70	1.7	20	96
13. [8]	D/2	4	1	4	$V_H/2$	$V_H/2$	$V_H/2$	$V_H/2$	300	100	0.3	20	94
14. [38]	$\frac{D}{1+D}$	3	1	4	$V_H - V_L$	$V_H - V_L$	$V_H - V_L$		42	14	0.12	30	96
<sup>a</sup> Schemotic with out o	بمططيبيه بمعيين												

"Schematic without current snubber. <sup>b1</sup>Topology from Figure 4 or 5. <sup>c1</sup>Topology implemented in one stage. <sup>d1</sup>Two level configuration with four switches;  $k = 4V_H - 3V_L$ .

TABLE 2 Comparison between the BHSI and other bidirectional topologies

Converter (x)	Voltage ratio $V_L/V_H$	Inductor energy $W_{LTot(x)}$	Capacitor energy $W_{CTot(x)}$	Total device stress $S_{(x)}$
1.Buck/boost	D	$\frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_i \cdot f \cdot V_H}$	$\frac{I_L \cdot V_L \cdot (8 \cdot V_H - 8 \cdot V_L + r_i \cdot V_H)}{16 \cdot r_v \cdot f \cdot V_H}$	$2 \cdot I_L \cdot V_H$
2. BHSI	$\frac{D}{2-D}$	idem 1.	$\frac{I_L \cdot V_L \cdot (V_H - V_L)}{2 \cdot r_p \cdot f \cdot V_H}$	$\frac{I_L \cdot (V_H + V_L)^2}{V_H}$
3. [20]	idem 2.	idem 1.	$\frac{I_L \cdot V_L \cdot (4 \cdot V_H - 4 \cdot V_L + r_i \cdot V_H)}{8 \cdot r_p \cdot f \cdot V_H}$	idem 2.
4. [14]	idem 2.	idem 1.	$\frac{I_L V_L (16 V_H^2 - 8 V_H V_L + 8 V_L^2 + r_i V_H (V_L + V_H))}{16 \cdot r_r \cdot f \cdot V_H \cdot (V_H + V_L)}$	idem 2.
5. [36]	idem 2.	idem 1.	idem 2.	$\frac{3 \cdot I_L \cdot (V_H + V_L)^2}{2 \cdot V_H}$
6. [37]	idem 2.	$\frac{I_L \cdot V_L \cdot (3V_H^2 - 2V_H \cdot V_L - V_L^2)}{4 \cdot r_i \cdot f \cdot V_H \cdot (V_H + V_L)}$	$\frac{I_L \cdot V_L \cdot (V_H - V_L + r_i \cdot (V_H + V_L)/16)}{r_p \cdot f \cdot (V_H + V_L)}$	idem 2.
7. [27]	$D^2$	$\frac{I_L \cdot V_L \cdot (V_H^{1/2} - V_L^{1/2})}{r_i \cdot f \cdot V_H^{1/2}}$	$\frac{I_L \cdot V_L \cdot (V_H^{1/2} - V_L^{1/2} + r_i \cdot V_H^{1/2}/16)}{r_v \cdot f \cdot V_H^{1/2}}$	$4 \cdot I_L \cdot V_H^{1/2} \cdot V_L^{1/2}$
8. [11]	idem 7.	idem 7.	idem 7.	idem 7.
9. [23]	idem 7.	idem 7.	idem 7.	idem 7.
10. [24]	idem 7.	idem 7.	$\frac{I_L \cdot V_L \cdot (V_H^{1/2} - V_L^{1/2})}{r_{\mathfrak{p}} \cdot f \cdot V_H^{1/2}}$	idem 7.
11. [9]	idem 7.	idem 7.	idem 7.	$I_L \cdot (2 \cdot V_H + 3 \cdot (V_H \cdot V_L)^{1/2})$
12. [17]	$\frac{D^2}{D^2 - D + 1}$	$W_{LTot(12)}^{a}$	W <sub>CTot</sub> (12) <sup>b</sup>	$\frac{2I_L V_L (V_H - V_L)^2 (k - V_L^{1/2} k^{1/2})}{V_H (2V_L^2 - 3V_H V_L + V_H V_L^{1/2} k^{1/2})}$
13. [8]	<i>D</i> /2	$\frac{I_L \cdot V_L \cdot (V_H - 2 \cdot V_L)}{2 \cdot r_i \cdot f \cdot V_H}$	$\frac{I_L \cdot V_L \cdot (V_H - V_L + r_i \cdot V_H / 16)}{r_p \cdot f \cdot V_H}$	$\frac{I_L \cdot V_H \cdot (V_H - V_L)}{V_H - 2 \cdot V_L}$
14. [38]	$\frac{D}{1+D}$	idem 13.	$\frac{I_{L} \cdot V_{L} \cdot (2V_{H}^{2} - 2V_{L} \cdot V_{H} + 2V_{L}^{2} + r_{i} \cdot (V_{H}^{2} - V_{L} \cdot V_{H}))}{8 \cdot r_{p} \cdot f \cdot V_{H} \cdot (V_{H} - V_{L})}$	$\frac{2 \cdot I_L \cdot \left(V_H - V_L\right)^3}{V_H \cdot \left(V_H - 2 \cdot V_L\right)}$

 $^{a}W_{LTdef(12)} = \frac{I_{\underline{L}} \cdot V_{\underline{L}} \cdot (640 \cdot V_{\underline{H}}^{2} \cdot V_{\underline{L}}^{2} + 5V_{\underline{L}}^{3/2} k^{5/2} + 14V_{\underline{L}}^{5/2} k^{3/2} - 3V_{\underline{L}}^{7/2} k^{1/2} - 192V_{\underline{H}} \cdot V_{\underline{L}}^{3} - 704V_{\underline{H}}^{3} \cdot V_{\underline{L}} + 256V_{\underline{H}}^{4} - 16V_{\underline{H}}^{2} \cdot V_{\underline{L}}^{1/2} k^{3/2} )}{256v_{\underline{L}} \cdot f \cdot V_{\underline{H}}^{2} \cdot (V_{\underline{H}} - V_{\underline{L}})^{2}}$ 

 ${}^{\mathrm{b}}W_{CTde(12)} = \frac{l_{L}V_{L}(2V_{H}^{2}k^{1/2} - 8V_{H}^{2}V_{L}^{1/2} - V_{L}^{2}k^{1/2} + 10V_{H}V_{L}^{3/2} - 3V_{L}^{5/2})}{2 \cdot r_{C} \cdot f \cdot V_{H} \cdot (V_{H}k^{1/2} - 3V_{H}V_{L}^{1/2} + 2V_{L}^{3/2})},$  where  $k = 4V_{H} - 3V_{L}$ .

Even though BHSI exposes a higher voltage on  $S_1$ , compared to a conventional bidirectional buck/boost converter, the total active switch stress is lower:

$$S = \frac{I_L \cdot (V_H + V_L)^2}{V_H}.$$
 (22)

#### 2.3 BHSI comparison to other topologies

In this section the BHSI is compared to other topologies, presented in the Appendix (Table 1), numbered from 1 to 14. For a more relevant comparison, only topologies that fall under the following conditions are chosen: with two and up to four transistors, without multiphase or multilevel topologies (as the BHSI and most topologies can be extended for multiphase operation), and without coupled inductors. The selected topologies are grouped based on their voltage conversion ratio: 1, a conventional buck/boost converter used as a reference; 2, the BHSI and; 3-6, converters with similar conversion ratio; 7-11, quadratic or; 12, similar converters, with higher voltage conversion ratio; 13-14, switched capacitor converters.

Basic characteristics of the topologies are presented in Table 1: voltage conversion ratio, number of components, maximum voltage stress on each switch, and the electrical specifications of the prototypes. The information from this table shows that the BHSI achieves a good conversion ratio with a reduced number of components, and even though it has a larger voltage stress acting on  $S_1$ , it performs very well in terms of efficiency when compared to other topologies.

The main comparison is performed based on the conversion ratio, total inductor or capacitor energy, and total active switch stress, information presented for all selected topologies in the Appendix (Table 2). The energy stored in passive components is used for comparison as it is proportional to the actual volume and costs of these components (the number of components alone does not characterize this aspect). Similarly, the total active switch stress is used to characterize the overall costs and losses in these devices. The relations from Table 2 are represented in Figures 5-8 for a more concise comparison.

All relations except the conversion ratio are normalized to the conventional buck/boost converter (1), as the  $r_i$  and  $r_v$  cancel out for the inductor energy and capacitor energy calculations, respectively. For the capacitive energy calculation,  $r_i$  is not eliminated, therefore, it was set to 20%, showing a small influence on the results.

In the conversion ratio comparison, in Figure 5, the BHSI is placed approximately in the middle, between the quadratic converters and the conventional converter. In this graph, the



**FIGURE 5** Conversion ratio comparison between the BHSI converter (2), conventional converter (1), and other state-of-the-art converters (3–14) presented in Table 2



**FIGURE 6** Total inductor energy comparison, between the BHSI converter (2) and other state-of-the-art converters (3–14) presented in Table 2 (values are normalized to the conventional converter (1) energy)



**FIGURE 7** Total capacitor energy comparison, between the BHSI converter (2) and other state-of-the-art converters (3–14) presented in Table 2 (values are normalized to the conventional converter (1) energy)



**FIGURE 8** Total active switch stress comparison, between the BHSI converter (2) and other state-of-the-art converters (3–14) presented in Table 2 (values are normalized to the conventional converter (1) energy)

step-down operation is considered because it can be easily compared for the entire range of the duty cycle, whereas for the boost operation the conversion ratio theoretically approaches infinity at larger duty cycles. If very wide conversion ratios are desired, the quadratic converters (i.e. 7–11) seem to be more appropriate, as they achieve better conversion ratios at lower duty cycles. Very low conversion ratios may not be necessarily desired in all SC applications (e.g. the application described in Section 4). Here, with a duty cycle of 10%,  $V_L$  decreases down to 5% of  $V_H$ , resulting in a sufficiently wide voltage range for the SC.

In terms of inductor energy comparison, the BHSI has the third best position as presented in Figure 6, placed after converters 13 and 14. Compared to the conventional buck/boost and converters 3–5, the BHSI has the same requirement for inductor energy, although it has two inductors.

Even though the output current of BHSI has a larger ripple (Figure 4), the total capacitor energy is small, the second smallest, together with 5, compared to the rest of the considered topologies, as shown in Figure 7.

In terms of total active device stress, the BHSI, and converters 3, 4, 6, and 13 have the best results over a wide range of conversion ratios, as illustrated in Figure 8. All converters except 11, and partially 5 and 12, have lower device stress compared to the conventional buck/boost.

Overall, the BHSI achieves very good performances. Converters 13 and 14 have competitive results, but they do not have a wide conversion ratio, being limited at a maximum of 50%. Apart from the limited conversion ratio, they have another disadvantage: the switched capacitors are connected in parallel at different voltages, and from this connection large currents might occur.

From the results presented in Figures 5–8 the BHSI is compared to the most relevant converters from Table 2 by using the radar charts from Figures 9 and 10. The information presented in these figures is an alternative for the overall



**FIGURE 9** BHSI (2) compared to similar voltage conversion ratio converters (6 and 13), for: voltage conversion ratio (D = 15%), mean inductor and capacitor energy, mean total active switch stress, and total number of switches



**FIGURE 10** BHSI (2) compared to wider voltage conversion ratio converters (7 and 12), for: voltage conversion ratio (D = 15%), mean inductor and capacitor energy, mean total active switch stress, and total number of switches

cost/volume/efficiency evaluation of the converter. The criterions used for comparison are the voltage conversion ratio at D = 15%, the averaged total inductor and capacitor energies, the averaged total active switch stress, and the total number of active switches (Sw. count). From Figure 9, where the BHSI is compared to similar voltage conversion ratios converters, 6 and 13, it is shown that the BHSI has best overall performances. In Figure 10, the BHSI is compared to the two wider voltage conversion ratio converters, 7 and 12. Apart for the wider voltage conversion ratio, the BHSI has better characteristics.

Depending on the application different converters can be chosen and, in general, the BHSI has good performances, making it a good candidate for wide range of applications.

## 3 | DYNAMIC MODELLING

In this section the dynamic modelling of the BHSI is described, which is used for stability analysis of the system and for the controller design.



**FIGURE 11** BHSI schematic used for dynamic analysis with parasitic resistances having values shown in Table 3



**FIGURE 12** BHSI equivalent schematic during *t<sub>on</sub>* interval, used for dynamic analysis

The state space representation of the two equivalent states of the circuit are written as:

$$\dot{x} = A_i \cdot x + B_i \cdot u, \tag{23}$$

where *i* is equal to 1 for the  $t_{on}$  state and 2 for  $t_{off}$ .

Considering equal currents for the two inductors, the state (x) and input vector (u) are, respectively, given by:

$$x = \begin{bmatrix} i_{L1} \\ v_{CH} \\ v_{CL} \end{bmatrix}, \quad u = \begin{bmatrix} V_H \\ V_L \end{bmatrix}.$$
(24)

The state  $(A_i)$  and input  $(B_i)$  matrices are, respectively:

$$A_{i} = \begin{bmatrix} a_{11_{i}} & a_{12_{i}} & a_{13_{i}} \\ a_{21_{i}} & a_{22_{i}} & 0 \\ a_{31_{i}} & 0 & a_{33_{i}} \end{bmatrix}, \quad B_{i} = \begin{bmatrix} b_{11_{i}} & b_{12_{i}} \\ b_{21_{i}} & 0 \\ 0 & b_{32_{i}} \end{bmatrix}.$$
(25)

The elements of the matrices are detailed in the Appendix and were calculated based on the BHSI schematic with inclusion of parasitic resistors, as presented in Figure 11. The two equivalent schematics which include the parasitic components for  $t_{on}$ and  $t_{off}$  states are presented in Figures 12 and 13, respectively.

In order to obtain the small signal model of the converter, small signal perturbations are applied to the variables in order



**FIGURE 13** BHSI equivalent schematic during  $t_{aff}$  interval, used for dynamic analysis

TABLE 3 BHSI dynamic model parameters

Element	Value	Unit	Element	Value	Unit
$V_H$	300	V	D	0.347	_
$V_L$	60	V	$r_H$	37.5	$\mathrm{m}\Omega$
$C_H$	1.98	mF	$r_L$	23.7	$\mathrm{m}\Omega$
$C_L$	4.23	mF	r <sub>CH</sub>	50	$\mathrm{m}\Omega$
L <sub>1</sub> , L <sub>2</sub>	100	$\mu H$	r <sub>CL</sub>	35.2	$\mathrm{m}\Omega$
Т	25	$\mu$ s	$r_{L1}, r_{L2}$	9	$\mathrm{m}\Omega$
$r_i$	0.3	—	$I_{L1}, I_{L2}$	30	А
$r_v$	0.02	_	$r_{S1}, r_{S2}, r_{S2}$	40	$\mathrm{m}\Omega$

to linearize the system:

$$x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad y = Y + \tilde{y}.$$
 (26)

The state vector, X, for steady-state operation,  $\dot{X} = 0$ , can be used for finding the relation between the input voltages,  $V_H$ and  $V_L$ , duty cycle, D, and the state vector elements, by also taking into consideration the parasitic elements. The state vector is calculated with:

$$X = -A_e^{-1} \cdot B_e \cdot u. \tag{27}$$

Considering the duty cycle as the input variable for the new linearized system, and the inductor current as the output variable, the system is described as:

$$\begin{cases} \dot{\tilde{x}} = A_e \cdot \tilde{x} + B_e \cdot \tilde{d} \\ \tilde{y} = C_e \cdot \tilde{x} \end{cases}$$
(28)

The equivalent matrices  $(A_e, B_e, C_e)$  are calculated as:

$$A_{e} = (A_{1} \cdot D + A_{2} \cdot (1 - D)),$$
  

$$B_{e} = ((A_{1} - A_{2}) \cdot X + (B_{1} - B_{2}) \cdot u),$$
  

$$C_{e} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}.$$
(29)

The values from Table 3 were designed using the relations from Section 2.2 and are used for calculating the control to out-



**FIGURE 14** Bode plots of BHSI models: continuous time model  $G_P(s)$ , ZOH discrete time conversion  $G_P(z)$ , ZOH discrete time conversion with additional delay  $P(z) \cdot G_P(z)$  and frequency response of the model simulation in PSIM

put transfer function:

$$G_P(s) = \frac{\tilde{y}}{\tilde{d}} = \frac{\tilde{i}_{L1}}{\tilde{d}},$$
(30)

$$G_P(s) = \frac{1.811 \cdot 10^6 \cdot s^2 + 1.722 \cdot 10^{10} \cdot s + 4.197 \cdot 10^{13}}{s^3 + 1.045 \cdot 10^4 \cdot s^2 + 3.027 \cdot 10^7 \cdot s + 1.87 \cdot 10^{10}}.$$
(31)

The Bode plot of the transfer function  $(G_p)$  is presented in Figure 14 for the continuous time together with the discretized transfer function. The discretization was realized using zero-order hold (ZOH) method, with the *T* representing the sampling time from Table 3.

In addition to the Bode plot obtained from the mathematical model, the open loop frequency response of the BHSI was also obtained through simulation using PSIM software. In this case, the simulation also included the microcontroller (MCU) used for the converter control, to have a more realistic comparison between the results. As seen in Figure 14, the simulation model and discretized model of the converter display a clear difference.

This difference is not only because of the analog to digital conversion (ADC), which is already taken into account by the ZOH method, but by the delay in the PWM update time.

The PWM delay time is added to the mathematical model using a first-order Padé approximation of a time delay equal to the switching period:

$$P(s) = \frac{-T \cdot s + 1}{T \cdot s + 1}.$$
(32)



**FIGURE 15** Open loop Bode plots of BHSI model with discrete controller  $G_C(z)$ , and frequency response of the model simulation in PSIM ( $PM = 68.5^\circ, f_c = 1.55 \text{ kHz}$ )



**FIGURE 16** Control loop structure, containing the controller,  $G_C(z)$ , the Padé approximation of PWM delay, P(s), and the linearized model of the BHSI,  $G_P(s)$  (discretized using the ZOH method)

The modified converter model consisting of the discretized transfer function, with added Padé approximation,  $P(z) \cdot G_P(z)$ , offers a better resemblance to the simulation model.

Based on the plot from Figure 14, a controller was designed to obtain (i) zero steady-state error, (ii) reduced overshoot, and (iii) fast transition between the two operating regimes. The controller was designed by directly shaping the Bode plot with the Control System Designer app from MATLAB, obtaining the following transfer function:

$$G_C = 5.4236 \cdot 10^{-3} \cdot \frac{z - 0.9802}{z - 1}.$$
 (33)

In Figure 15 the open loop response of the controller with the converter model is presented. The phase margin (PM) of the system is 68.5°, at the cutoff frequency  $(f_c)$  of 1.55 kHz. The gain margin (GM) of the system is 13.8 dB at 6.76 kHz. The simulation model, which also includes the MCU, was used to confirm the mathematical model. The complete structure of the control loop is presented in Figure 16.

**TABLE 4** BHSI prototype parameters

Element	Value	Unit
$V_H$	300	V
$V_L$	60	V
$C_H$	1.98	mF
$C_L$	4.23	mF
$L_1, L_2$	100	$\mu { m H}$
f	40	kHz
P <sub>in</sub>	3	kW
Si-MOSFETs	3x IXFK80N60P3	
GaN-FETs	3x TPH3207WS	



FIGURE 17 Experimental test setup for the BHSI

## 4 | EXPERIMENTAL RESULTS

#### 4.1 | BHSI operation

Two experimental prototypes were built using two types of transistors: conventional Si-MOSFETs (IXFK80N60P3) and GaN-FETs (TPH3207WS). The passive components are sized according to Table 4 for both prototypes, with approximately 20% less electrolytic capacitors for the GaN prototype, where larger ceramic capacitors were used because of the faster switching times. Even though the selected devices could achieve higher switching frequencies, the same value (40 kHz) was used for both prototypes in order to achieve better efficiencies which are required for SC storage applications.

For this topology it is important to manage the voltage oscillations that appear on the inductors during  $t_{on}$  (i.e. when the two are connected in series), an aspect which was analysed in the unidirectional topology in [30]. The initial voltage spike appears because of the tolerances of the two inductances, and is theoretically limited by a maximum of two times the nominal voltage, as can be observed from Figure 2. The voltage on the inductor oscillates because of the resonant circuit created by the inductors and the parasitic capacitors of  $S_2$  and  $S_3$  switches during  $t_{on}$ . Based on [30], similar methods can be further proposed for the BHSI for eliminating the voltage oscillations. A passive RC snubber (231  $\Omega$  and 4.7 nF) was used in parallel to one of the two inductors in order to dampen the voltage oscillations.

The experimental setup, presented in Figure 17, was built to test the operation of the BHSI in both operating modes (buck and boost), offering the possibility of a fast transition between



**FIGURE 18** Steady-state results of MOSFET prototype: simulations (left) and experimental (right);  $I_{L1} = 10$  (A)



**FIGURE 19** Steady-state results of GaN-FET prototype: simulations (left) and experimental (right);  $I_{L1} = 10$  (A)

the two. The setup contains two supercapacitors (BMOD0063 P125 B04) on the low voltage side ( $V_L$ ), and a combination of a DC source and a constant voltage load, on the high voltage side ( $V_H$ ), with the purpose of emulating a DC voltage bus.

The purpose of the experiment is to demonstrate the BHSI operation as a bidirectional interface between SC storage and a DC microgrid bus, and to validate the stability for the transition between the two operation modes. Because the energy stored in the SC is proportional to its squared voltage, it is essential for the converter to operate over a wide voltage range, with a wide voltage conversion ratio, an aspect which is also verified experimentally.

Experimental and simulation results include steady state and transient results for both prototypes, showing a very similar operation.

Steady-state operation results are presented in Figures 18 and 19 for the MOSFET and GaN prototypes, respectively. The two sets of results are very similar, even though simulation results show smaller inductor voltage oscillations for the GaN



**FIGURE 20** Transient response results of MOSFET prototype: simulations (left) and experimental (right);  $I_{L1} = \pm 20$  (A)



**FIGURE 21** Transient response results of MOSFET prototype: simulations (left) and experimental (right);  $I_{L1} = \pm 20$  (A)

prototype because of smaller parasitic  $C_{ds}$  capacitances. The difference in the experimental operation is mainly because of other parasitic capacitances that are not accounted for, such as voltage probe parasitic capacitances, capacitance between traces, heatsink and transistor case. The inductor currents also present small oscillations, which are insignificant compared to the average currents.

Transient response results show the operation of the two prototypes for different current references,  $\pm 20$  A for Figures 20 and 21,  $\pm 10$  A for Figures 22 and 23, illustrating a fast transition between the two operation modes, and no difference between the two prototypes. The two different prototypes show that the control structure is independent of the prototype. All results were obtained with the converter operating around the nominal voltage values,  $V_L = 60$  V and  $V_H = 300$  V.

In order to demonstrate the wide voltage ratio capability of the BHSI, charge/discharge tests of the SC were performed



**FIGURE 22** Transient response results of GaN-FET prototype: simulations (left) and experimental (right)  $I_{L1} = \pm 10$  (A)



**FIGURE 23** Transient response results of GaN-FET prototype: simulations (left) and experimental (right)  $I_{L1} = \pm 10$  (A)

with constant current control. The  $V_L$  voltage was varied in Figure 24 from a minimum voltage of 7.7 V to a maximum of 77 V, resulting in a voltage conversion ratio  $(V_L/V_H)$  varying from 2.6% to 26%. A constant inductor current of  $I_{L1} = \pm 17.6$ A was maintained, resulting in a SC current of  $I_L \approx \pm 30$  A and the power varied between 0.3 to 2 kW. The same experiment was performed for larger  $I_{L1}$  currents of  $\pm 23.4$  A  $(I_L \approx \pm 42$  A) in Figure 25, where the  $V_L$  voltage was varied from a voltage of 9.3 to 51 V, resulting in a voltage conversion ratio varying from 3% to 17%. Another advantage is also visible from the presented results: a larger  $I_L$  output current compared to the inductor current, which is also demonstrated in (4).

The experimental results prove a stable operation for both step-down and step-up operation modes, with a fast transition between them. Bidirectional operation is required for an efficient SC storage interface for both charging and discharging. A wide voltage operation range is also tested, the converter being able to reduce its conversion ratio as low as 2.6%, a feature



**FIGURE 24** SC charge/discharge with  $I_L \approx \pm 30$  (A),  $I_{L1} = \pm 17.6$ (A),  $V_L = 7.7-77$  (V),  $V_L/V_H = 2.6-26$  (%),  $P_{in} = 0.3-2$  (kW)

which is usually difficult to achieve, but important in order to have a good utilization of the SC energy.

#### 4.2 | Efficiency results

The efficiency of the two prototypes was analysed using mathematical and experimental approaches, with the results shown in Figures 26-30.

The experimental efficiency was calculated by measuring the input and output currents and voltages, with a power of up to 3 kW.

The theoretical efficiency was calculated from the losses of the parasitic resistances from Figure 11 and the switching losses of the transistors. The switching loss calculation was performed according to [35]. Apart from efficiency, the transistor junction temperature and power loss distributions are also calculated.

Based on these results, significant advantages can be observed for the GaN prototype in terms of efficiency, in both operating modes, having an increase in efficiency of 2% in buck mode and 5% in boost mode.

The analytical description and the experimental results are in good correspondence for the buck operating mode but present a difference in the boost mode (5% for MOSFET and 3% for GaN). The difference can be caused by a few factors, such as



**FIGURE 25** SC charge/discharge with  $I_L \approx \pm 42$  (A),  $I_{L1} = \pm 23.4$  (A),  $V_L = 9.3-51$  (V),  $V_L/V_H = 3-17$  (%),  $P_{in} = 0.4-2$  (kW)



**FIGURE 26** Efficiency and switch temperatures for the MOSFET prototype, in buck (left) and boost mode (right)

different turn-on delay between  $S_2$  and  $S_3$ , a higher dv/dt on  $S_1$  during  $S_2 - S_3$  turn-on, or larger voltages on  $S_2$  and  $S_3$  during their turn-off, possibly resulting in shoot-through.

From the power distribution on the switches, presented in Figures 27 and 29, it can be concluded that the losses of the GaN devices are approximately 30% of that of the MOSFET



**FIGURE 27** Power loss distributions for the MOSFET prototype, in buck (left) and boost mode (right)



FIGURE 28 Efficiency and switch temperatures for the GaN prototype, in buck (left) and boost mode (right)

devices. The remaining power losses are distributed in the passive components as shown in Figure 30, and are considered identical for both prototypes.

The two BHSI prototypes are presented in Figures 31 and 32, for MOSFET and GaN, respectively. Since the same switching frequency was used in order to achieve higher efficiency for both prototypes, the size of the passive components for the two prototypes is considered the same, with small differences in the layout of the components. A major difference is observed in the heatsink which has a reduced volume for the GaN transistors, as they have smaller losses.

Overall, the BHSI achieves a very good efficiency compared to other topologies presented in Table 1, which is an important characteristic for the renewable energy applications where the SC storage is usually implemented.



FIGURE 29 Power loss distributions for the GaN prototype, in buck (left) and boost mode (right)



FIGURE 30 Power loss distributions from the passive components, similar for both prototypes

## 5 | CONCLUSION

In this paper, a BHSI was presented. Analytical description, operation, stability analysis, and efficiency estimations were validated through digital simulations and experimentally for the two prototypes.

The advantages of the proposed topology include a wider voltage conversion ratio, smaller passive components, lower active device stress, all based on the addition of the switched inductor cell. Even with the introduction of an additional inductor, the new topology does not introduce additional states in the control system, remaining a lower order system, compared to other wide ratio converters, giving it a further advantage. This paper also presents a thorough comparison between the proposed topology and other topologies presented in the scientific literature, highlighting the advantages of the BHSI.



FIGURE 31 BHSI prototype with MOSFET transistors (IXFK80N60P3)



FIGURE 32 BHSI prototype with GaN transistors (TPH3207WS)

The dynamic analysis is performed, and a control scheme is developed. The mathematical model for the dynamic operation presented in this paper can be successfully used for analysing any new BHSI prototypes.

The experimental results on the two prototypes using Si-MOSFET and GaN-FET, respectively, confirmed the theoretical findings. The theoretical and experimental efficiency results confirm the advantages of the GaN switches.

Few disadvantages of the topology, such as the high frequency voltage between inputs and inductor voltage oscillations represent topics to be resolved in future work.

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#### **CONFLICT OF INTEREST**

The authors declare no conflict of interest.

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#### APPENDIX

The elements of  $A_1$  matrix from (23), corresponding to  $t_{on}$  state, are:

$$a_{11_1} = -\frac{r_{L1} + \frac{r_{S1}}{2} + \frac{r_{CH} \cdot r_H}{2 \cdot (r_{CH} + r_H)} + \frac{r_{CL} \cdot r_L}{2 \cdot (r_{CL} + r_L)}}{L_1},$$

$$a_{12_1} = \frac{r_H}{2 \cdot L_1 \cdot (r_{CH} + r_H)} \ a_{13_1} = \frac{-r_L}{2 \cdot L_1 \cdot (r_{CL} + r_L)}$$

$$a_{21_1} = \frac{-r_H}{C_H \cdot (r_{CH} + r_H)} \quad a_{22_1} = \frac{-1}{C_H \cdot (r_{CH} + r_H)}$$
$$a_{31_1} = \frac{r_L}{C_L \cdot (r_{CL} + r_L)} \quad a_{33_1} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}.$$

The elements of  $B_1$  matrix from (23), corresponding to  $t_{on}$  state, are:

$$b_{11_1} = \frac{r_{CH}}{2 \cdot L_1 \cdot (r_{CH} + r_H)} \quad b_{12_1} = \frac{-r_{CL}}{2 \cdot L_1 \cdot (r_{CL} + r_L)},$$
$$b_{21_1} = \frac{1}{C_H \cdot (r_{CH} + r_H)} \quad b_{32_1} = \frac{1}{C_L \cdot (r_{CL} + r_L)}.$$

The elements of  $A_2$  matrix from (23), corresponding to  $t_{off}$  state, are:

$$a_{11_2} = -\frac{r_{L1} + r_{S2} + \frac{2 \cdot r_{CL} \cdot r_L}{(r_{CL} + r_L)}}{L_1}$$
$$a_{12_2} = 0 \quad a_{13_2} = \frac{-r_L}{L_1 \cdot (r_{CL} + r_L)},$$
$$a_{21_2} = 0 \quad a_{22_2} = \frac{-1}{C_H \cdot (r_{CH} + r_H)},$$
$$a_{31_2} = \frac{2 \cdot r_L}{C_L \cdot (r_{CL} + r_L)} \quad a_{33_2} = \frac{-1}{C_L \cdot (r_{CL} + r_L)}.$$

The elements of  $B_2$  matrix from (23), corresponding to  $t_{off}$  state, are:

$$b_{11_2} = 0 \ b_{12_2} = \frac{-r_{CL}}{L_1 \cdot (r_{CL} + r_L)},$$
  
$$b_{21_2} = \frac{1}{C_H \cdot (r_{CH} + r_H)} \ b_{32_2} = \frac{1}{C_L \cdot (r_{CL} + r_L)}.$$